AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

Listing Of Claims:

1. (Currently Amended) A multilayer wiring board comprising a plurality of insulating layers, a plurality of conductive layers, a conductive non-through hole for electrically connecting the plurality of conductive layers to each other, and a capacitor produced by forming electrodes on upper and lower surfaces of at least one insulating layer containing a high-dielectric material, wherein the capacitor is in an arbitrary layer except for a core layer and a layer structure is asymmetrical, a warpage is 4.0 x 10^{-4}mm^{-1} or less in curvature at a room temperature, and a hardened material of the high-dielectric material has a specific inductive capacity ranging from 20 to 100 at 25°C, 1 MHz and a thickness ranging from 0.1 to 30 μm.

2. (Cancelled).

3. (Currently Amended) The multilayer wiring board according to ~~claims~~ claim 1 ~~or 2~~, wherein the capacitor is in an arbitrary layer except for a core layer and a layer structure is asymmetrical, and a warpage is 1 mm or less.

4. (Currently Amended) A multilayer wiring board comprising a plurality of insulating ~~layer~~layers, a plurality of conductive layers, a conductive non-through hole for electrically connecting the plurality of conductive layers to each other, and a capacitor produced by forming electrodes on upper and lower surfaces of at least

one insulating layer containing a high-dielectric material, wherein an insulating material different from the high-dielectric material is filled in a recessed portion between conductive patterns including the electrodes, and the surfaces of the conductive patterns and the surface of the filled insulating material are planarized.

5. (Original) The multilayer wiring board according to claim 4, wherein the conductive pattern including at least one of the electrodes is in contact with different insulating materials of three types including the high-dielectric material.

6. (Currently Amended) A multilayer wiring board comprising a plurality of insulating layers, a plurality of conductive layers, a conductive hole for electrically connecting the plurality of conductive layers to each other, and a capacitor comprising at least one of the insulating layers containing a high-dielectric material having a specific inductive capacity ranging from 20 to 100 at 25°C, 1 MHz and produced by forming electrodes on upper and lower surfaces of the insulating layer, wherein at least one side of the counter electrodes has a thickness ranging from 1 to 18 μm and is arranged inside an outer periphery of the electrode opposing the electrode having the thickness.

7. (Cancelled).

8. (Currently Amended) The multilayer wiring board according to claim 6 ~~or 7~~, wherein a minimum horizontal distance between each side surface of the electrode having the thickness ranging from 1 to 18 μm and each side surface of the electrode opposing it are respectively ranging from 50 to 100 μm.

9. (Currently Amended) The multilayer wiring board according to ~~claims~~ claim 6 ~~to 8~~, wherein a minimum horizontal distance between each side surface of the electrode having the thickness ranging from 1 to 18 μm and an outer edge of the conductive hole formed on the electrode for electrically connecting arbitrary conductive layers are respectively 100 μm or more.

10. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~claim 6 ~~to 9~~, wherein the electrode having the thickness ranging from 1 to 18 μm is formed by etching and removing an unnecessary portion of a conductive layer.

11. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~claim 4 ~~to 10~~, wherein the capacitor is in an arbitrary layer except for a core layer, and a fluctuation in capacitance of the capacitor is less than ±5%.

12. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~ claim 1 ~~to 11~~, comprising an inductor formed by patterning at least one conductive layer.

13. (Original) The multilayer wiring board according to claim 12, wherein a thickness of the conductive layer in which the inductor is formed is smaller than a thickness of another conductive layer and ranges from 1 to 12 μm.

14. (Currently Amended) The multilayer wiring board according to claim 12 ~~or 13~~, wherein the inductor is manufactured on any one of the electrodes formed on the upper and lower surfaces of the insulating layer.

15. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~ claim 1 ~~to 14~~, comprising a non-through hole which simultaneously penetrates at least one of the insulating layer containing the high-dielectric material and another insulating layer adjacent to the insulating layer containing the high-dielectric material.

16. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~ claim 1 ~~to 15~~, wherein the high-dielectric material contains an epoxy resin, a hardening agent for the epoxy resin, and a high-dielectric material filler.

17. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~ claim 1 ~~to 16~~, wherein the high-dielectric material contains an epoxy resin, a hardening agent for the epoxy resin, a high-dielectric material filler, and a high-molecular-weight resin having at least one functional group and a weight-average molecular weight ranging from 10000 to 800000.

18. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~ claim 1 ~~to 17~~, wherein a melting viscosity of the high-dielectric material in a B-stage state at 120°C preferably ranges from 100 to 200 Pa·S.

19. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~ claim 16 ~~to 18~~, wherein the high-dielectric material filler is at least one selected from the group consisting of barium titanate, strontium titanate, calcium titanate, magnesium titanate, lead titanate, titanium dioxide, barium zirconate, and calcium zirconate, lead zirconate.

20. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~ claim 16 ~~to 19~~, wherein the high-dielectric filler is compounded 300 to 3000 parts by weight to the epoxy resin of 100 parts by weight.

21. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~ claim 1 ~~to 20~~, wherein, as an outermost conductive layer, at least one conductive pattern having a width of 300 μm or more is formed, and a thickness of an insulating layer adjacent to the outermost conductive layer is 150 μm or more.

22. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~claim 1 ~~to 21~~, wherein an insulating layer except for at least one of the insulating layers containing the high-dielectric material is reinforced by a glass substrate and contains an inorganic filler.

23. (Currently Amended) The multilayer wiring board according to ~~any one of claims~~ claim 1 ~~to 22~~, wherein the electrodes formed on the upper and lower surfaces of the insulating layer are formed so that one surface or both the surfaces of the insulating layer may not be entirely covered.

24. (Original) A manufacturing method of a multilayer wiring board which includes a plurality of insulating layers, a plurality of conductive layers, a conductive non-through hole for electrically connecting the plurality of conductive layers to each other, and a capacitor produced by forming electrodes on upper and lower surfaces of at least one insulating layer containing a high-dielectric material, comprising: at least

the step of forming conductive patterns including one of the electrodes;

the step of filling and hardening an insulating material different from the high-dielectric material in a recessed portion between the conductive patterns;

the step of planarizing the surfaces of the conductive patterns and the surface of the insulating material filled and hardened in the recessed portion between the conductive patterns by polishing; and

the step of heating and laminating a metal foil having the high-dielectric material in a semi-hardened state.

25. (Original) The manufacturing method of a multilayer wiring board according to claim 24, further comprising a step of forming a conductive pattern including the other of the electrodes by etching the metal foil.

26. (Original) The manufacturing method of a multilayer wiring board which includes a plurality of insulating layers, a plurality of conductive layers, a conductive hole for electrically connecting the plurality of conductive layers to each other, and a capacitor comprising at least one of the insulating layers containing a high-dielectric material having a specific inductive capacity ranging from 20 to 100 at 25°C, 1 MHz and produced by forming electrodes on upper and lower surfaces of the insulating

layer, wherein, in formation of a conductive pattern, the same substrate is exposed a plurality of times such that a pattern exposure area of a photosensitive resist is set at 1 to 250 cm^2/time.

27. (Original) The manufacturing method of a multilayer wiring board according to claim 26, wherein the electrode has a thickness ranging from 1 to 18 μm, and exposure is performed the plurality of times in formation of the conductive pattern including the electrode.

28. (Currently Amended) The manufacturing method of a multilayer wiring board according to claim 26 ~~or 27~~, wherein a photomask consisting of an inorganic material is used in pattern exposure of the photosensitive resist.

29. (Currently Amended) The manufacturing method of a multilayer wiring board according to ~~any one of claims~~ claim 26 ~~to 28~~, wherein the conductive pattern including the electrode is formed by etching and removing an unnecessary portion of a conductive layer.

30. (Currently Amended) The manufacturing method of a multilayer wiring board according to ~~any one of claims~~ claim 24 ~~to 29~~, further comprising the step of forming an inductor in at least one of the conductive layers.

31. (Currently Amended) A semiconductor device wherein a semiconductor chip is mounted on a multilayer wiring board according to ~~any one of~~

~~claims~~claim 1 ~~to 23 or a multilayer wiring board manufactured by a manufacturing method according to any one of claims 24 to 30~~.

32. (Original) A wireless electronic device wherein a semiconductor device according to claim 31 is mounted.

33. (New) The multilayer wiring board according to claim 8, wherein a minimum horizontal distance between each side surface of the electrode having the thickness ranging from 1 to 18 μm and an outer edge of the conductive hole formed on the electrode for electrically connecting arbitrary conductive layers are respectively 100 μm or more.

34. (New) The multilayer wiring board according to claim 8, wherein the electrode having the thickness ranging from 1 to 18 μm is formed by etching and removing an unnecessary portion of a conductive layer.

35. (New) The multilayer wiring board according to claim 9, wherein the electrode having the thickness ranging from 1 to 18 μm is formed by etching and removing an unnecessary portion of a conductive layer.

36. (New) The multilayer wiring board according to claim 6, wherein the capacitor is in an arbitrary layer except for a core layer, and a fluctuation in capacitance of the capacitor is less than ±5%.

37. (New) The multilayer wiring board according to claim 4, comprising an inductor formed by patterning at least one conductive layer.

38. (New) The multilayer wiring board according to claim 6, comprising an inductor formed by patterning at least one conductive layer.

39. (New) The multilayer wiring board according to claim 4, comprising a non-through hole which simultaneously penetrates at least one of the insulating layer containing the high-dielectric material and another insulating layer adjacent to the insulating layer containing the high-dielectric material.

40. (New) The multilayer wiring board according to claim 6, comprising a non-through hole which simultaneously penetrates at least one of the insulating layer containing the high-dielectric material and another insulating layer adjacent to the insulating layer containing the high-dielectric material.

41. (New) The multilayer wiring board according to claim 4, wherein the high-dielectric material contains an epoxy resin, a hardening agent for the epoxy resin, and a high-dielectric material filler.

42. (New) The multilayer wiring board according to claim 6, wherein the high-dielectric material contains an epoxy resin, a hardening agent for the epoxy resin, and a high-dielectric material filler.

43. (New) The multilayer wiring board according to claim 4, wherein the high-dielectric material contains an epoxy resin, a hardening agent for the epoxy resin, a high-dielectric material filler, and a high-molecular-weight resin having at least one functional group and a weight-average molecular weight ranging from 10000 to 800000.

44. (New) The multilayer wiring board according to claim 6, wherein the high-dielectric material contains an epoxy resin, a hardening agent for the epoxy resin, a high-dielectric material filler, and a high-molecular-weight resin having at least one functional group and a weight-average molecular weight ranging from 10000 to 800000.

45. (New) The multilayer wiring board according to claim 4, wherein a melting viscosity of the high-dielectric material in a B-stage state at 120°C preferably ranges from 100 to 200 Pa·S.

46. (New) The multilayer wiring board according to claim 6, wherein a melting viscosity of the high-dielectric material in a B-stage state at 120°C preferably ranges from 100 to 200 Pa·S.

47. (New) The multilayer wiring board according to claim 4, wherein, as an outermost conductive layer, at least one conductive pattern having a width of 300 μm or more is formed, and a thickness of an insulating layer adjacent to the outermost conductive layer is 150 μm or more.

48. (New) The multilayer wiring board according to claim 6, wherein, as an outermost conductive layer, at least one conductive pattern having a width of 300 μm or more is formed, and a thickness of an insulating layer adjacent to the outermost conductive layer is 150 μm or more.

49. (New) The multilayer wiring board according to claim 4, wherein an insulating layer except for at least one of the insulating layers containing the high-dielectric material is reinforced by a glass substrate and contains an inorganic filler.

50. (New) The multilayer wiring board according to claim 6, wherein an insulating layer except for at least one of the insulating layers containing the high-dielectric material is reinforced by a glass substrate and contains an inorganic filler.

51. (New) The multilayer wiring board according to claim 4, wherein the electrodes formed on the upper and lower surfaces of the insulating layer are formed so that one surface or both the surfaces of the insulating layer may not be entirely covered.

52. (New) The multilayer wiring board according to claim 6, wherein the electrodes formed on the upper and lower surfaces of the insulating layer are formed so that one surface or both the surfaces of the insulating layer may not be entirely covered.

53. (New) The manufacturing method of a multilayer wiring board according to claim 26, further comprising the step of forming an inductor in at least one of the conductive layers.

54. (New) A semiconductor device wherein a semiconductor chip is mounted on a multilayer wiring board according to claim 4.

55. (New) A wireless electronic device wherein a semiconductor device according to claim 54 is mounted.

56. (New) A semiconductor device wherein a semiconductor chip is mounted on a multilayer wiring board according to claim 6.

57. (New) A wireless electronic device wherein a semiconductor device according to claim 56 is mounted.

58. (New) A semiconductor device wherein a semiconductor chip is mounted on a multilayer wiring board manufactured by a manufacturing method according to claim 24.

59. (New) A wireless electronic device wherein a semiconductor device according to claim 58 is mounted.

60. (New) A semiconductor device wherein a semiconductor chip is mounted on a multilayer wiring board manufactured by a manufacturing method according to claim 26.

61. (New) A wireless electronic device wherein a semiconductor device according to claim 60 is mounted.